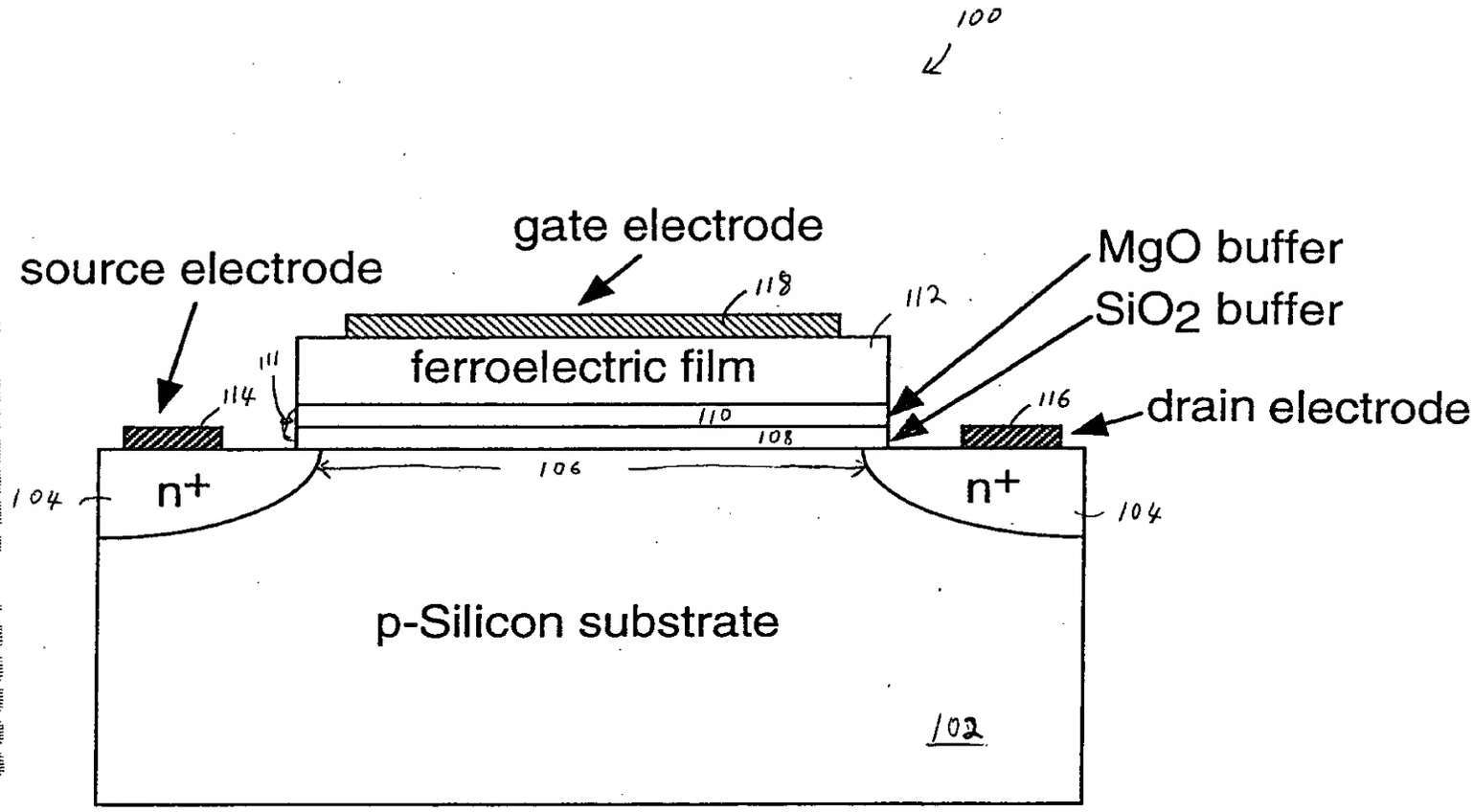
100
gate electrode
source electrode
MgO buffer
SiO2 buffer
118
112
ferroelectric film
111
114
110
108
116
drain electrode
106
n+
n+
104
104
p-Silicon substrate
102

FIG. 1

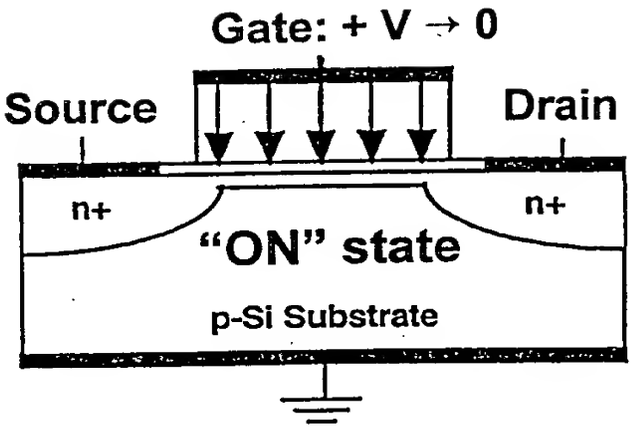
Gate: + V → 0
Source
Drain
n+
n+
"ON" state
p-Si Substrate

FIG. 2

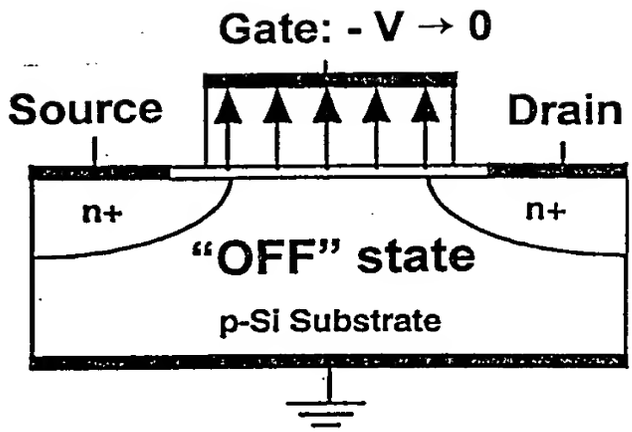
Gate: - V → 0
Source
Drain
n+
n+
"OFF" state
p-Si Substrate

FIG. 3

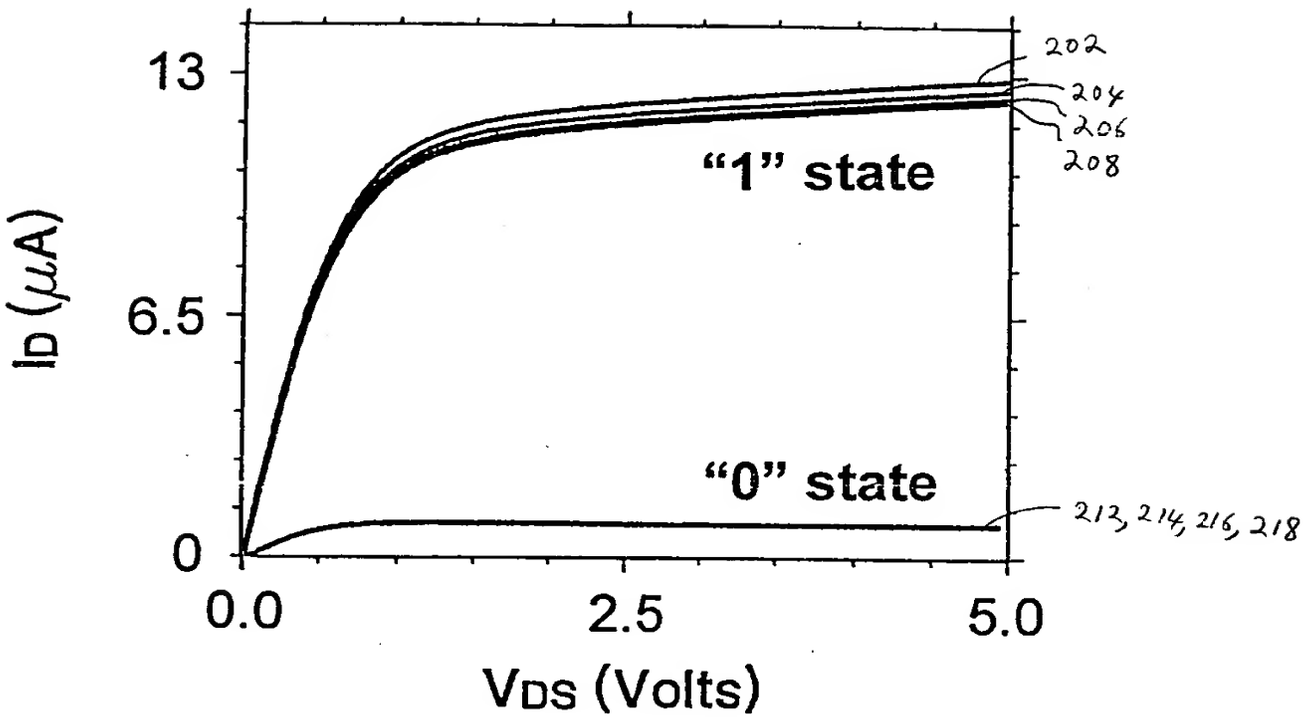
13
6.5
0
0.0
2.5
5.0
ID (μA)
VDS (Volts)
"1" state
"0" state
202
204
206
208
213, 214, 216, 218

FIG. 4

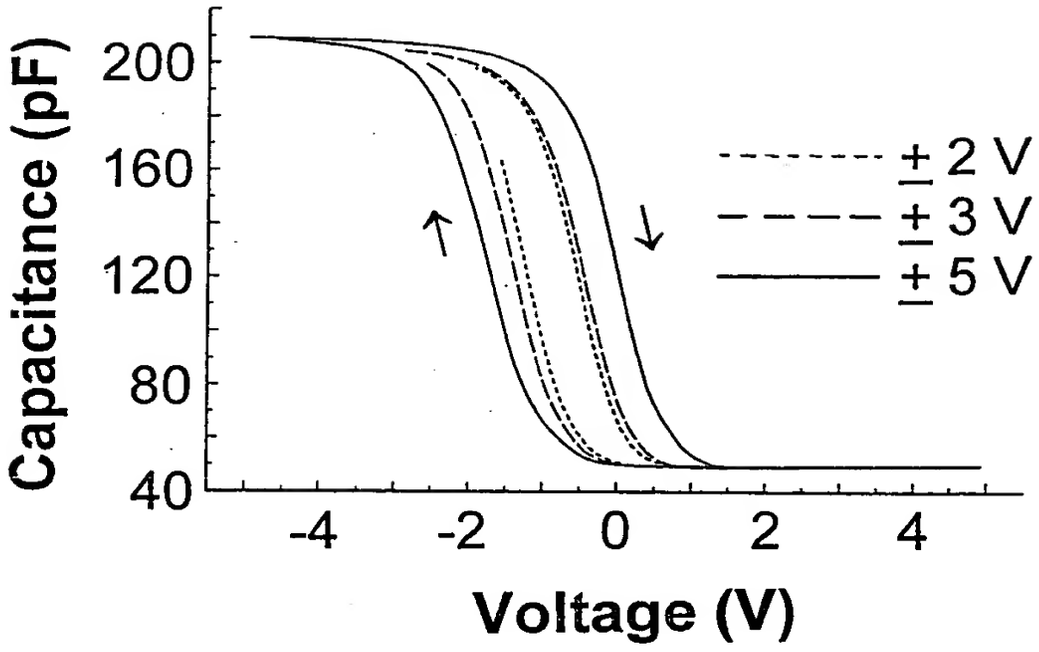

FIG. 5

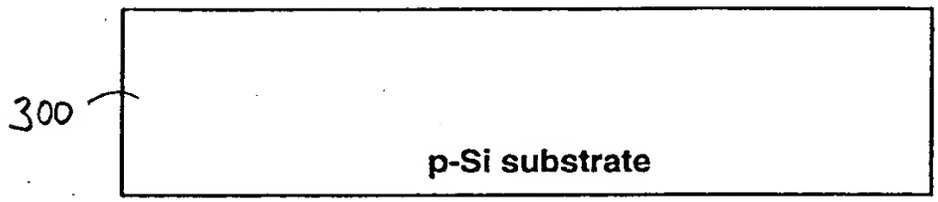

FIG. 6

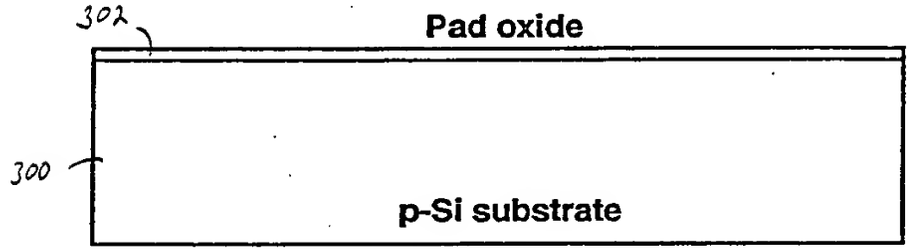

FIG. 7

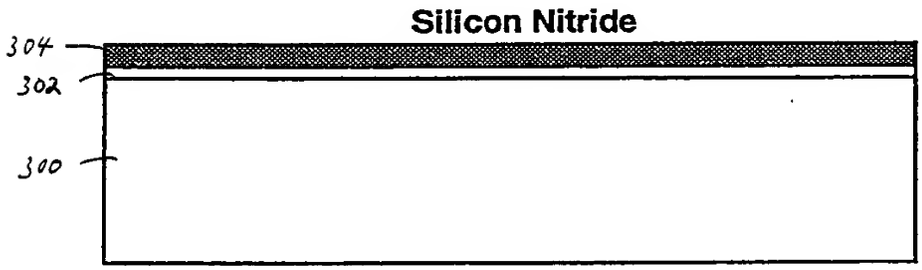

FIG. 8

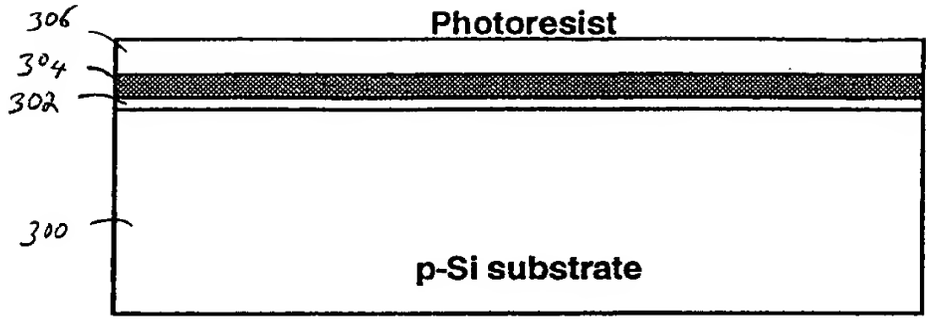

FIG. 9

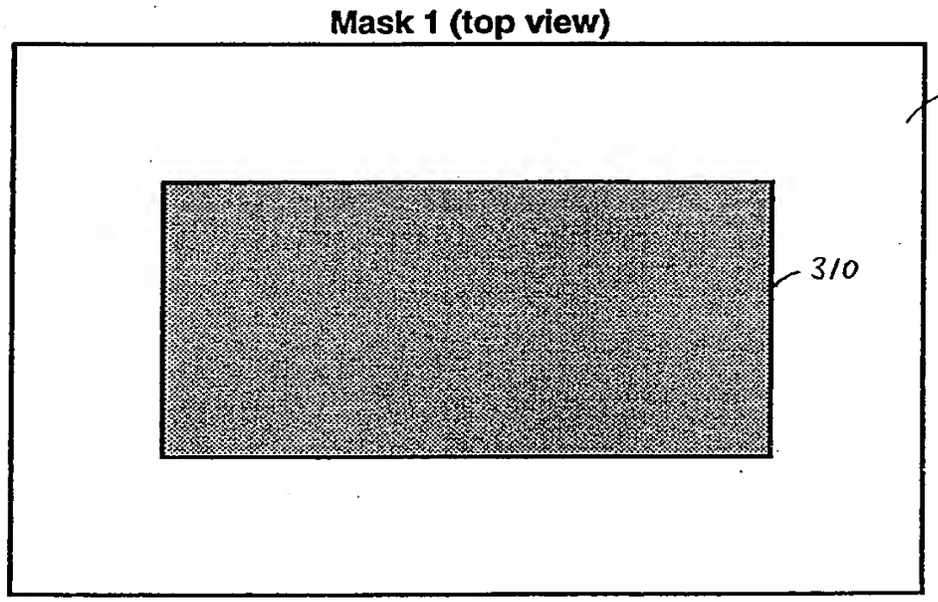

FIG. 10A

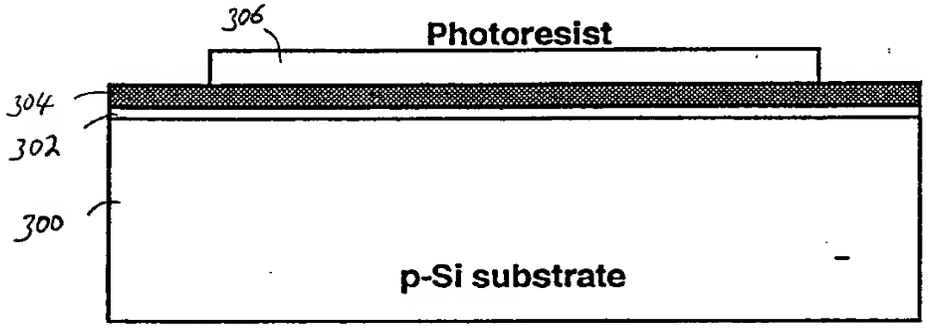

FIG. 10B

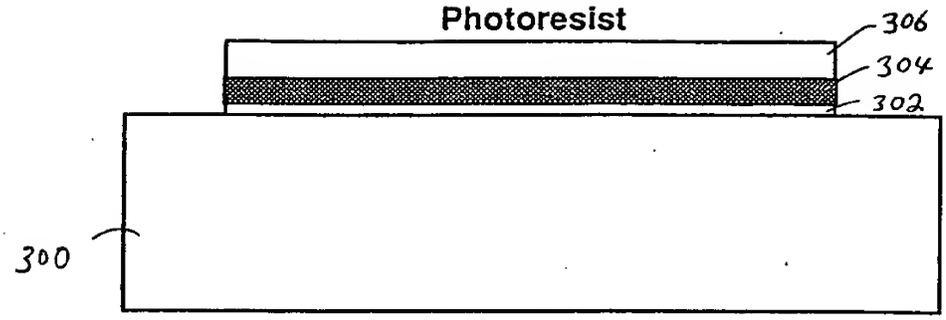

FIG. 11

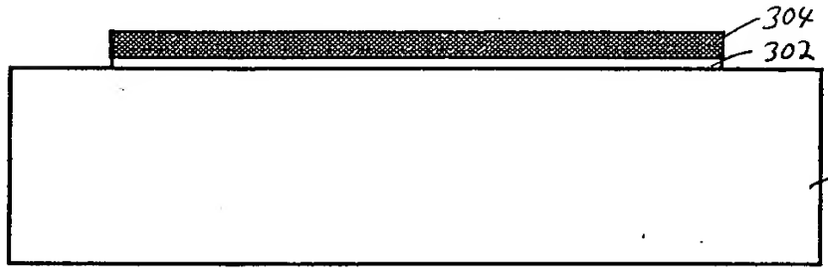

FIG. 12

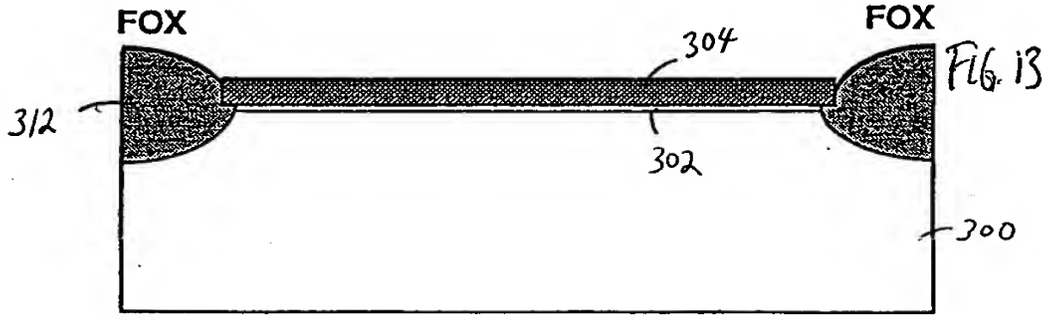

FIG. 13

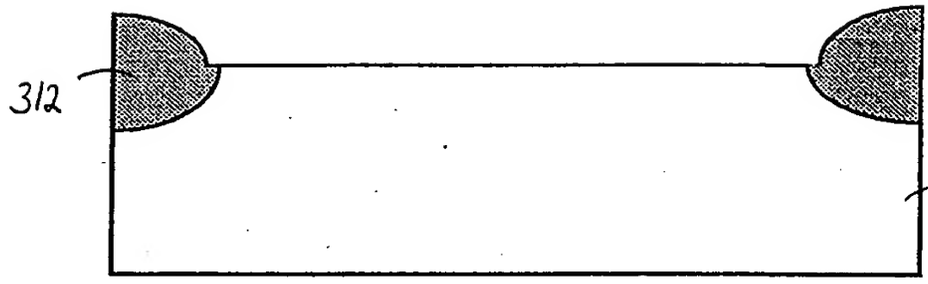

Fig. 14

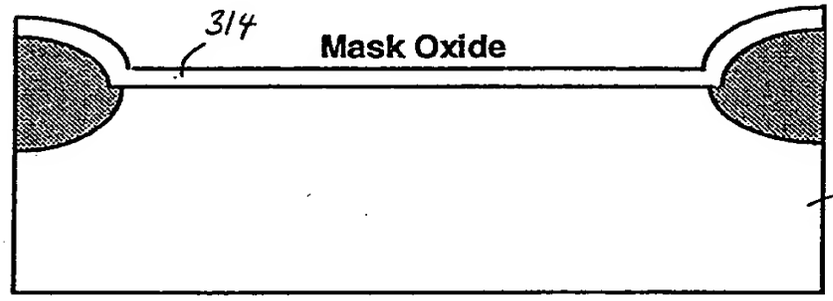

Fig. 15

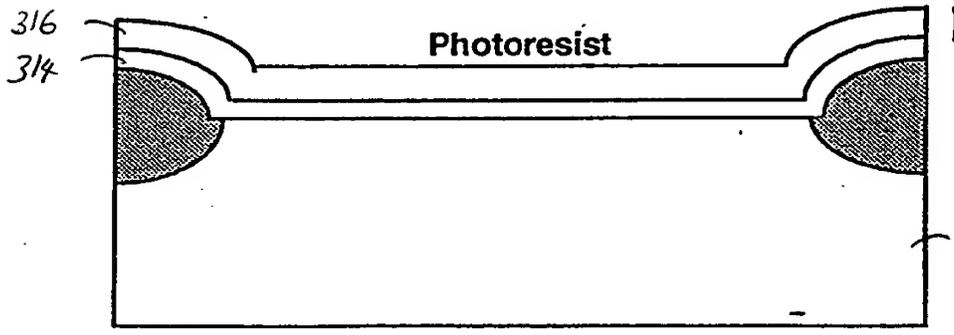

Fig. 16

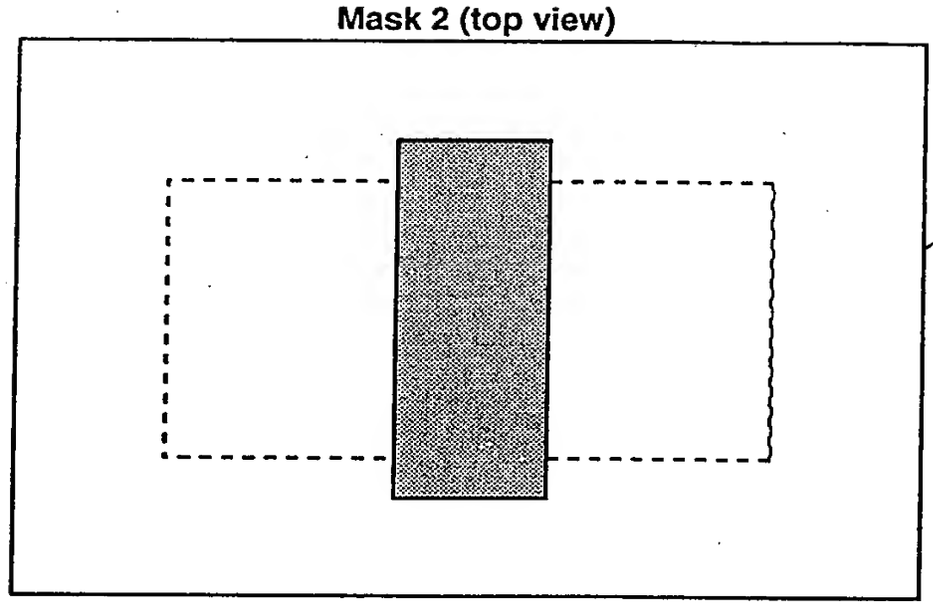

FIG. 17A

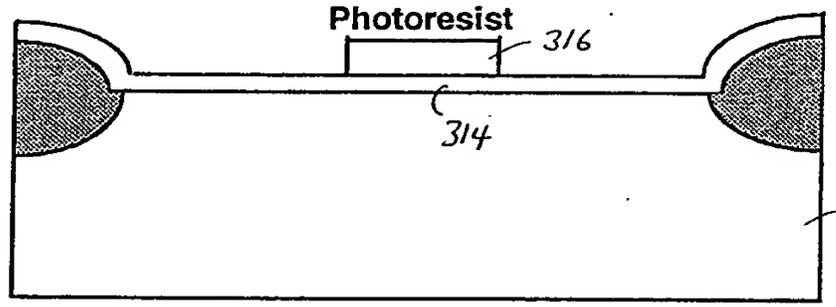

FIG. 17 B

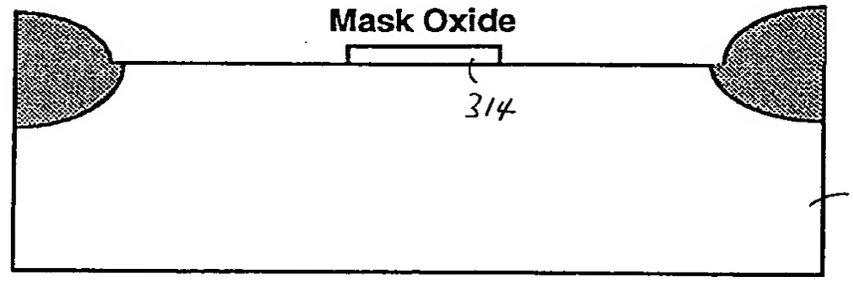

FIG. 17C

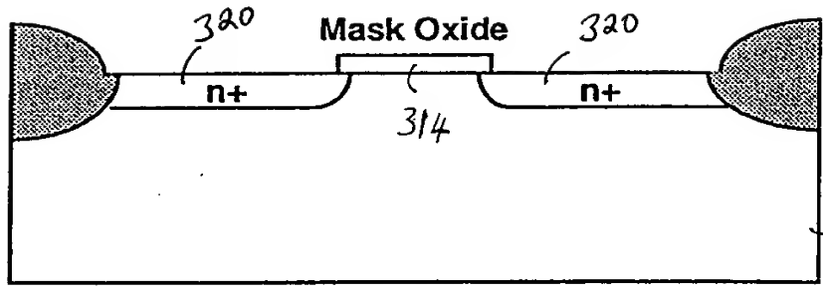

Fig. 19

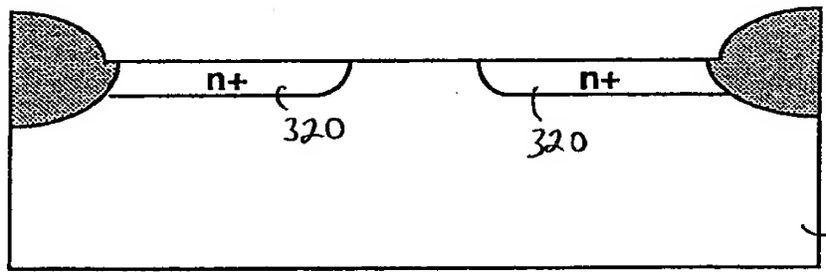

Fig. 20

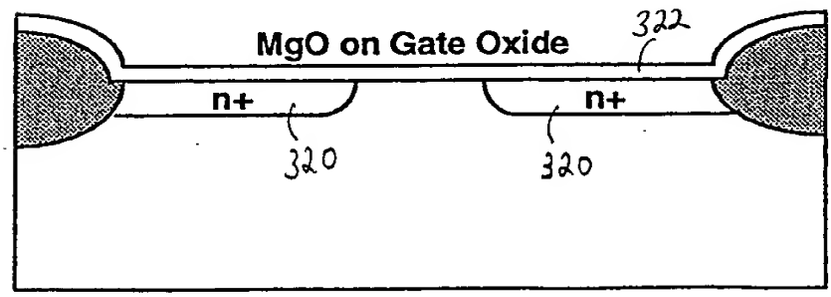

Fig. 21

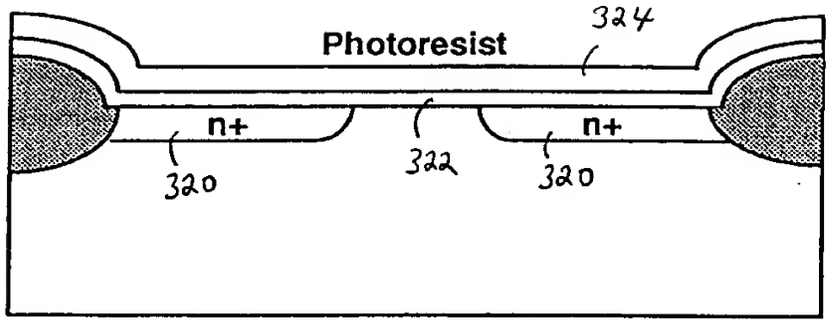

FIG. 22

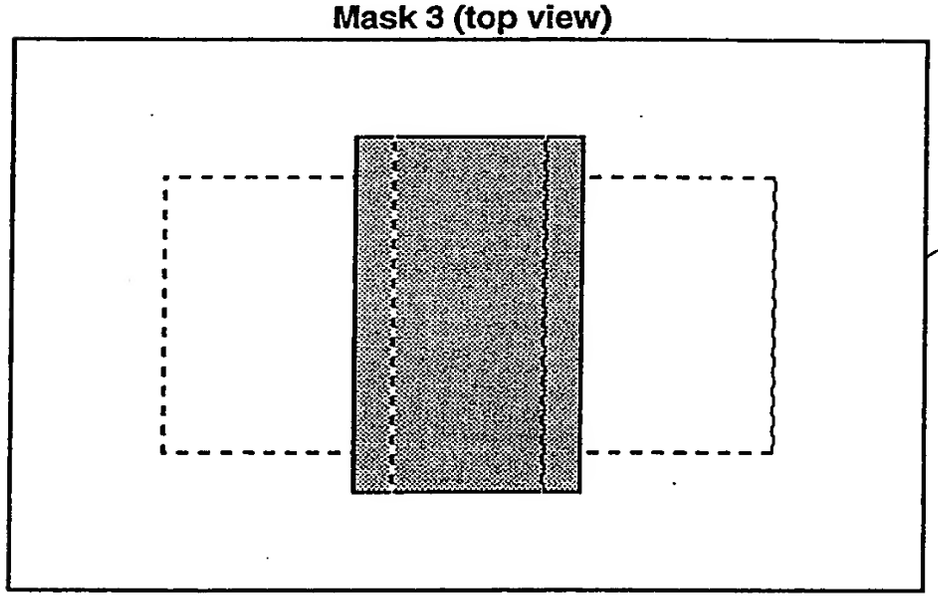

FIG. 23A

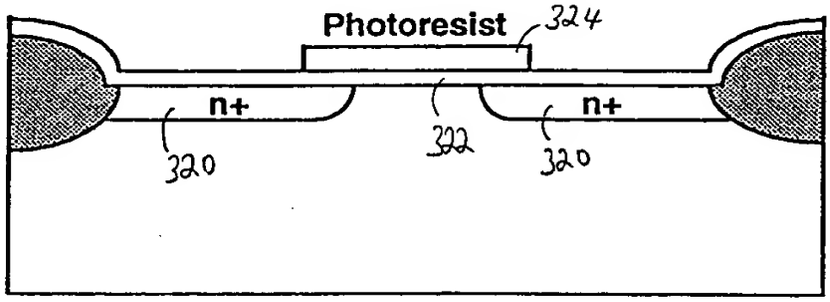

FIG. 23B

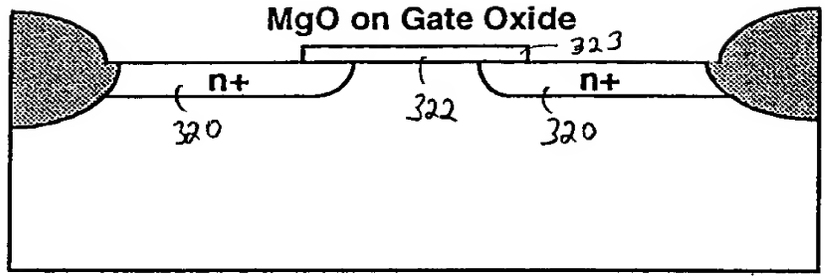

FIG. 24

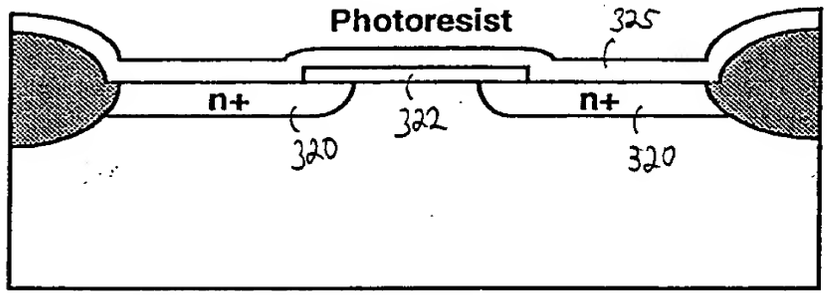

FIG. 25

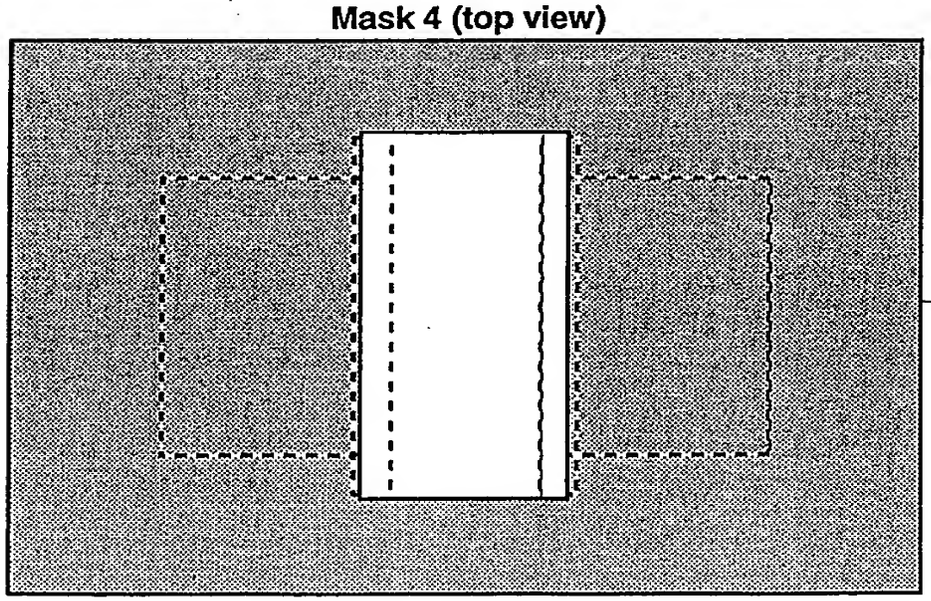

FIG. 26A

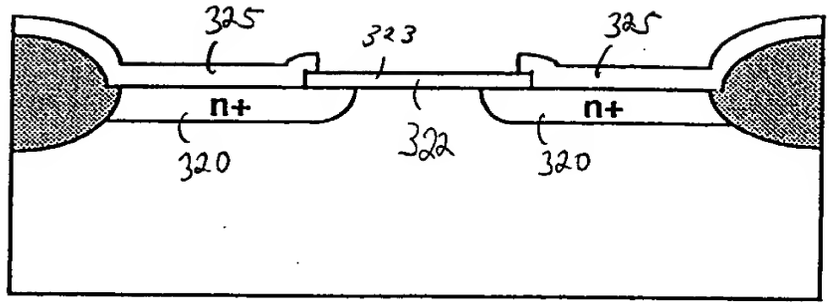

Fig. 26B

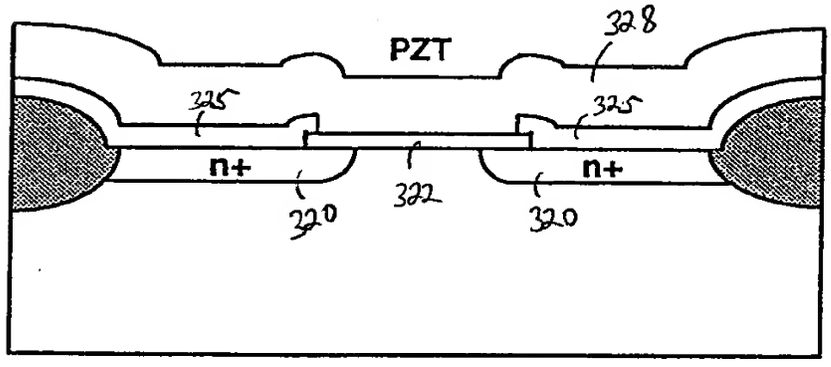

Fig. 27

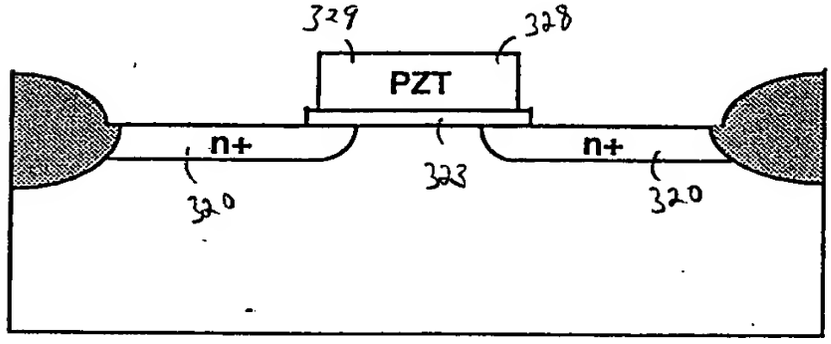

Fig. 28

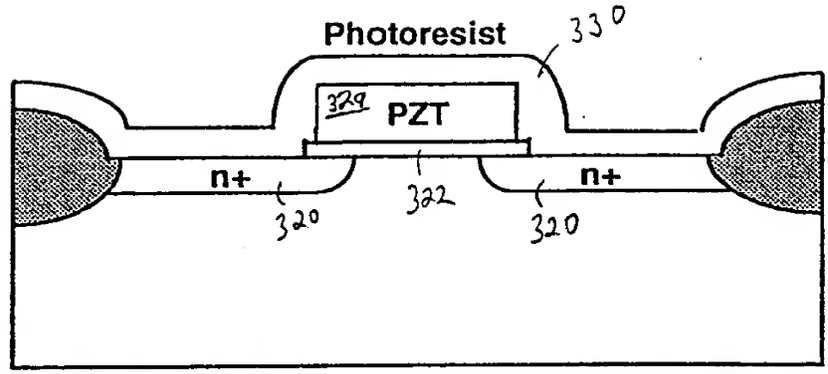

FIG. 29

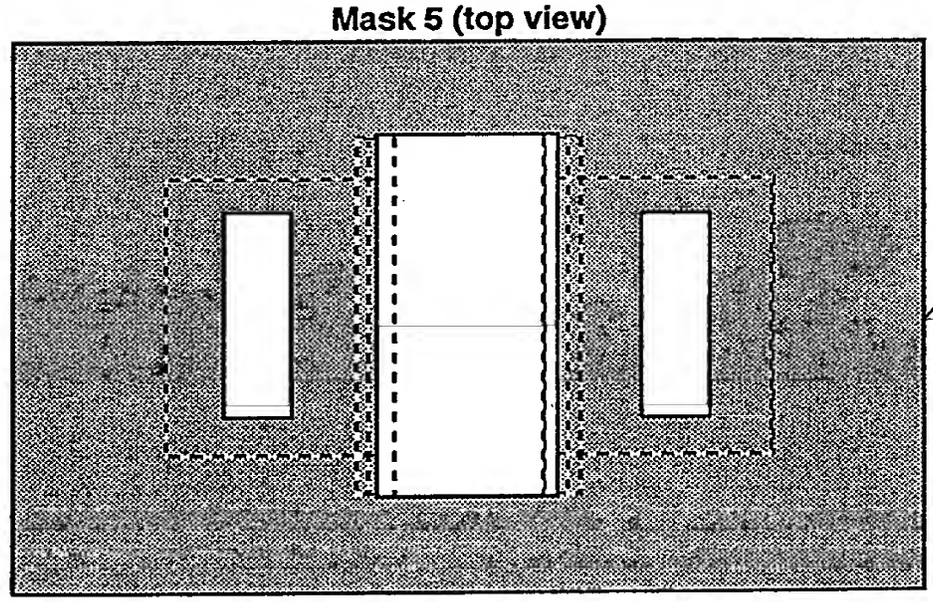

FIG. 30A

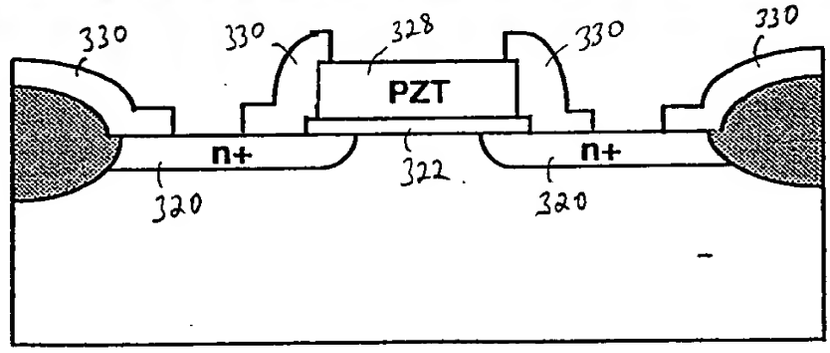

FIG. 30B

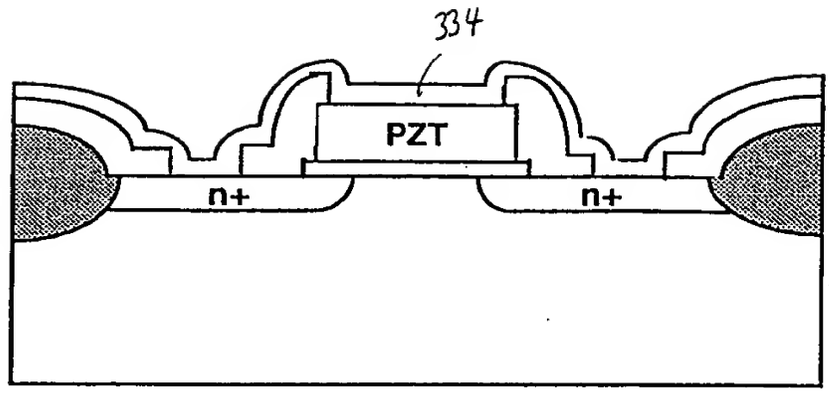
334
PZT
n+
n+

Fig. 31

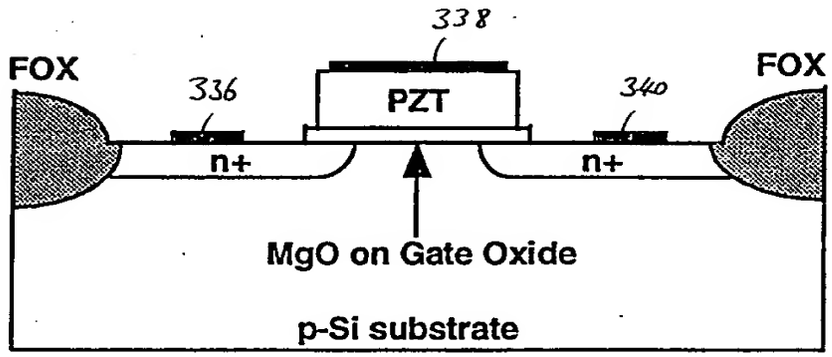
338
FOX
336
PZT
340
FOX
n+
n+
MgO on Gate Oxide
p-Si substrate

Fig. 32

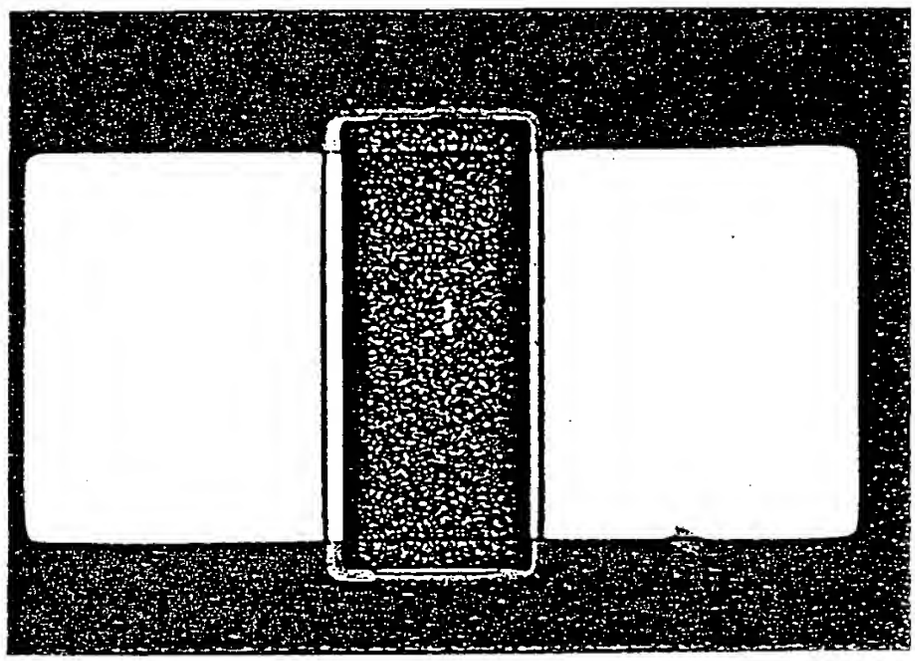

FIG. 33